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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,231	01/31/2002	Wayne D. Kever	10016695-1	4653

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EXAMINER	
KOMOL, VAJIRACHAI	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,231	KEVER ET AL.	
	Examiner	Art Unit	
	Vajirachai Komol	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-5, 7-9, 11-12, 14-16, 18-19, 21-23, 25-26, 28-30, 32-33, 35-37, 39-40, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houston [U.S. Pat. 5,615,162] in the view of Mittal et al [U.S. Pat. 5,719,800].

Regarding to claim 1, Houston teaches a circuit for applying power to an on-chip cache memory array [col. 5 lines 66-67] comprising:

- a switch [26, fig. 2 or similar switches in other figures] in series with a power supply and said on-chip cache memory array [col. 5, lines 65 – 67, col. 6, lines 49 – 52];
- a software application [col. 4, lines 49 – 52];
- wherein said switch may be opened or closed [col. 3, lines 15 – 20].

Houston does not teach a Performance Monitor Unit [PMU]. Specifically, Houston uses control signals to control the opening and closing of switch 26. However, Houston does not detail the circuitry for generating the control signals.

Mittal et al teach the circuitry for generating the cache memory power control signal. Specifically, Mittal et al teach a PMU [fig. 3] which is electrically connected to

the on-chip cache memory array and generates the cache memory power control signals [col. 9, lines 5 – 48]. Mittal et al also teach that the PMU is controlled by a software application [col. 9, lines 65 – 66].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Houston and Mittal et al because they both directed to the teaching of controlling the power consumption of a on-chip cache memory array and Mittal et al teach the details of the control unit which is missing in Houston system.

Regarding to claim 2, Houston further teaches switching device is connected between a negative terminal of said on-chip cache memory array and GND of said power supply [col. 6, lines 35 - 36].

Regarding to claim 4, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 5, Houston further teaches switching device is connected between a positive terminal of said on-chip cache memory array and VDD of said power supply [col. 2, lines 58 - 61 and fig. 1].

Regarding to claim 7, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37-38].

Regarding to claim 8, Houston teaches a circuit for applying power to an on-chip cache memory array [col. 5 lines 66-67] comprising:

- a switch [26, fig. 2 or similar switches in other figures] in series with a power supply and said on-chip cache memory array [col. 5, lines 65 – 67, col. 6, lines 49 – 52];
- wherein said switch may be opened or closed [col. 3, lines 15 – 20].

Houston does not teach a Performance Monitor Unit [PMU]. Specifically, Houston uses control signals to control the opening and closing of switch 26. However, Houston does not detail the circuitry for generating the control signals.

Mittal et al teach the circuitry for generating the cache memory power control signal. Specifically, Mittal et al teach a PMU [fig. 3] which is electrically connected to the on-chip cache memory array and generates the cache memory power control signals [col. 9, lines 5 – 48].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Houston and Mittal et al because they both directed to the teaching of controlling the power consumption of a on-chip cache memory array and Mittal et al teach the details of the control unit which is missing in Houston system.

Regarding to claim 9, Houston further teaches switching device is connected between a negative terminal of said on-chip cache memory array and GND of said power supply [col. 6, lines 35 - 36].

Regarding to claim 11, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 12, Houston further teaches switching device is connected between a positive terminal of said on-chip cache memory array and VDD of said power supply [col. 2, lines 58 - 61 and fig. 1].

Regarding to claim 14, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 15, Houston teaches a circuit for applying power to an on-chip cache memory array [col. 5 lines 66-67] comprising:

- a switch [26, fig. 2 or similar switches in other figures] in series with a power supply and said on-chip cache memory array [col. 5, lines 65 – 67, col. 6, lines 49 – 52];
- a software application [col. 4, lines 49 – 52];
- wherein said switch may be opened or closed [col. 3, lines 15 – 20].

Houston does not teach a Performance Monitor Unit [PMU]. Specifically, Houston uses control signals to control the opening and closing of switch 26. However, Houston does not detail the circuitry for generating the control signals.

Mittal et al teach the circuitry for generating the cache memory power control signal. Specifically, Mittal et al teach a PMU [fig. 3] which is electrically connected to the on-chip cache memory array and generates the cache memory power control signals [col. 9, lines 5 – 48]. Mittal et al also teach that the PMU is controlled by a software application [col. 9, lines 65 – 66].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Houston and Mittal et al because they both directed to the teaching of controlling the power consumption of a on-chip cache memory array and Mittal et al teach the details of the control unit which is missing in Houston system.

Regarding to claim 16, Houston further teaches switching device is connected between a negative terminal of said on-chip cache memory array and GND of said power supply [col. 6, lines 35 - 36].

Regarding to claim 18, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 19, Houston further teaches switching device is connected between a positive terminal of said on-chip cache memory array and VDD of said power supply [col. 2, lines 58 - 61 and fig. 1].

Regarding to claim 21, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 22, Houston teaches a circuit for applying power to an on-chip cache memory array [col. 5 lines 66-67] comprising:

- electrically connecting a switch [26, fig. 2 or similar switches in other figures] between a power supply and said on-chip cache memory array [col. 5, line 65 – 67, col. 6, lines 49 – 52];
- a software application [col. 4, lines 49 – 52];
- wherein said switch may be opened or closed [col. 3, lines 15 – 20].

Houston does not teach a Performance Monitor Unit [PMU]. Specifically, Houston uses control signals to control the opening and closing of switch 26. However, Houston does not detail the circuitry for generating the control signals.

Mittal et al teach the circuitry for generating the cache memory power control signal. Specifically, Mittal et al teach a PMU [fig. 3] which is electrically connected to the on-chip cache memory array and generates the cache memory power control signals [col. 9, lines 5 – 48]. Mittal et al also teach that the PMU is controlled by a software application [col. 9, lines 65 – 66].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Houston and Mittal et al because they both directed to the teaching of controlling the power consumption of a on-chip cache memory

array and Mittal et al teach the details of the control unit which is missing in Houston system.

Regarding to claim 23, Houston further teaches switching device is connected between a negative terminal of said on-chip cache memory array and GND of said power supply array [col. 6, lines 35 - 36].

Regarding to claim 25, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 26, Houston further teaches switching device is connected between a positive terminal of said on-chip cache memory array and VDD of said power supply [col. 2, lines 58 - 61 and fig. 1].

Regarding to claim 28, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 29, Houston teaches a circuit for applying power to an on-chip cache memory array [col. 5 lines 66-67] comprising:

- electrically connecting a switch [26, fig. 2 or similar switches in other figures] between a power supply and said on-chip cache memory array [col. 5, line 65 – 67, col. 6, lines 49 – 52];
- wherein said switch may be opened or closed [col. 3, lines 15 – 20].

Houston does not teach a Performance Monitor Unit [PMU]. Specifically, Houston uses control signals to control the opening and closing of switch 26. However, Houston does not detail the circuitry for generating the control signals.

Mittal et al teach the circuitry for generating the cache memory power control signal. Specifically, Mittal et al teach a PMU [fig. 3] which is electrically connected to the on-chip cache memory array and generates the cache memory power control signals [col. 9, lines 5 – 48].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Houston and Mittal et al because they both directed to the teaching of controlling the power consumption of a on-chip cache memory array and Mittal et al teach the details of the control unit which is missing in Houston system.

Regarding to claim 30, Houston further teaches switching device is connected between a negative terminal of said on-chip cache memory array and GND of said power supply array [col. 6, lines 35 - 36].

Regarding to claim 32, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 33, Houston further teaches switching device is connected between a positive terminal of said on-chip cache memory array and VDD of said power supply [col. 2, lines 58 - 61 and fig. 1].

Regarding to claim 35, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 36, Houston teaches a circuit for applying power to an on-chip cache memory array [col. 5 lines 66-67] comprising:

- electrically connecting a switch [26, fig. 2 or similar switches in other figures] between a power supply and said on-chip cache memory array [col. 5, line 65 – 67, col. 6, lines 49 – 52];
- a software application [col. 4, lines 49 – 52];
- wherein said switch may be opened or closed [col. 3, lines 15 – 20].

Houston does not teach a Performance Monitor Unit [PMU]. Specifically, Houston uses control signals to control the opening and closing of switch 26. However, Houston does not detail the circuitry for generating the control signals.

Mittal et al teach the circuitry for generating the cache memory power control signal. Specifically, Mittal et al teach a PMU [fig. 3] which is electrically connected to the on-chip cache memory array and generates the cache memory power control signals [col. 9, lines 5 – 48]. Mittal et al also teach that the PMU is controlled by a software application [col. 9, lines 65 – 66].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Houston and Mittal et al because they both directed to the teaching of controlling the power consumption of a on-chip cache memory

array and Mittal et al teach the details of the control unit which is missing in Houston system.

Regarding to claim 37, Houston further teaches switching device is connected between a negative terminal of said on-chip cache memory array and GND of said power supply array [col. 6, lines 35 - 36].

Regarding to claim 39, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

Regarding to claim 40, Houston further teaches switching device is connected between a positive terminal of said on-chip cache memory array and VDD of said power supply [col. 2, lines 58 - 61 and fig. 1].

Regarding to claim 42, Houston further teaches switching device is a bipolar transistor [col. 6, lines 37 - 38].

8. Claims 3, 6, 10, 13, 17, 20, 24, 27, 31, 34, 38, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houston [U.S. Pat. 5,615,162] in the view of Mittal et al [U.S. Pat. 5,719,800] and further in view of Noda [U.S. Pat. 6,498,762].

Regarding to claims 3, 6, 10, 13, 17, 20, 24, 27, 31, 34, 38, and 41 as set forth above, Houston and Mittal et al teach all the limitations of claims 1-2, 5, 8-9, 12, 15-16,

19, 22-23, 26, 29-30, 33, 36-37, and 40. However, neither Houston nor Mittal et al teach the switching device is a MOSFET.

Noda discloses an internal power switch MOSFET [col. 2, line 5].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Houston, Mittal et al and Noda because they all directed to the teaching of controlling the power consumption in order to reduce the subthreshold leakage current and Noda teaches the details of the power switch MOSFET which is missing in Houston and Mittal et al systems.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vajirachai [Ben] Komol whose telephone number is (571) 272-5858. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VK

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